Study and Fabrication of MIOS Memory Structure

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ABSTRACT

This research represents fabrication and investigation for various kinds of MIOS structures as memorization devices. All structures were fabricated with dot and strip gates. The analysis is based on an investigation of charge transport in the Al_2O_3/SiO stacked films. It was shown that the trap-assisted tunneling is the dominant conduction mechanism through Al_2O_3 layer and is responsible for charge trapping into Al_2O_3 or Al_2O_3/SiO interface and into the second insulator layer. Nonvolatile digital memory switching has been observed in MIOS prepared by thermal vacuum thin film deposition.

دراسة وتصنيع تركيبة ذاكرة خزن نوع(MIOS)

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الخلاصة

يعنى هذا البحث بتصنيع ودراسة و تقصي احتمالية استخدام تراكيب (MIOS) معدن-عازل-أوكسيد-شبه موصل كنبائط ذاكرة. إن جميع التراكيب المصنعة استخدمت نوعين من البوابات، بوابة من نوع dot وأخرى من نوع strip .أن التحليل يعتمد على تقصي انتقال الشحنات في الطبقة المتراكبة من العوازل Al_2O_3/SiO. وقد تبين أن ميكانيكية التوصيل خلال Al_2O_3 هي المسؤولة عن عملية التنفيق وقنص الشحنات يكون في الطبقة البينية بين العازلين وفي الطبقات العازلة.لقد أظهرت التراكيب(MIOS) المصنعة والمحضرة بتقنية الترسيب الفراغي الحراري إمكانية استخدامها كخلايا للخزن المنطقي الدائمي.

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Introduction:

The memory devices are structures whose resistance and capacitance vary with magnitude and polarity of applied voltages [1]. The storage devices may be volatile or nonvolatile. They can be used as an analog or digital memory. The MOS structure is an important type of the memory devices. Recently the shunt capacitances of such structures have been studied and investigated thoroughly [2, 3]. The retention and endurance of charges in the non-volatile memories depend on the oxide layer of the device. The oxide layer is the most important part in the MOS structure. This layer limits the type of the storage device. The MOS device is essential structure in flash EEPROM memory. It is more important to study the factors and parameters which influence switching and retention of memorization in MIOS structures. The different types of fabricated structures have been studied as storage cells memories. The examined MIOS structures with (I-V) measurements show the switching operation between ON and OFF states and back to original state by inverting the polarity of the applied bias voltage. This process is verified in first and second deposited structures. The (C-V) measurements show the storage capability of the device by noting variety of capacitance values. Also the shifting operation was noted with applying the suitable stress for a certain time. This is verified in the last fabricated structure. In addition, all structures have been fabricated with two kinds of gate, dot and strip. The capacitances in the different gates are variable. After applying the stresses, the shifting in the original curve is known as shifting window.

Device Fabrication:

Fabrication procedures for the tested devices are illustrated in the following subsection

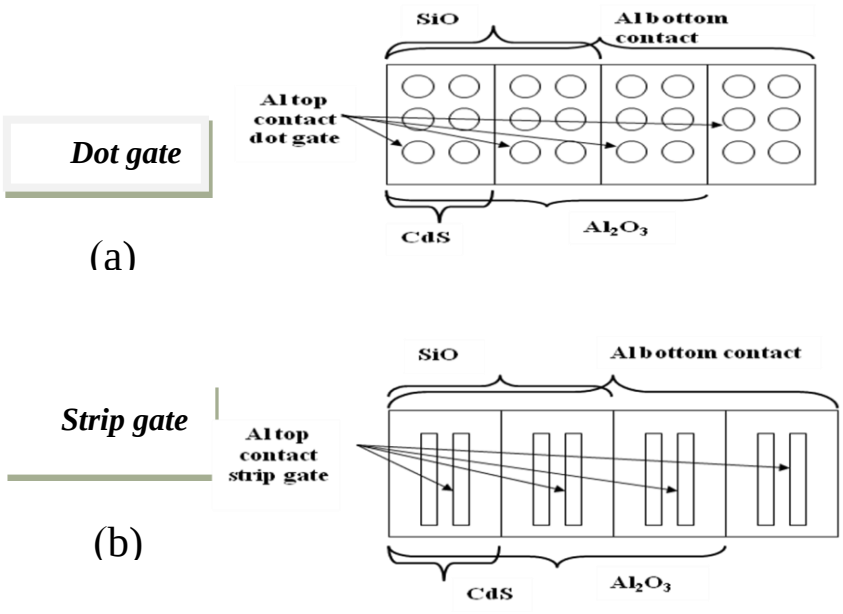
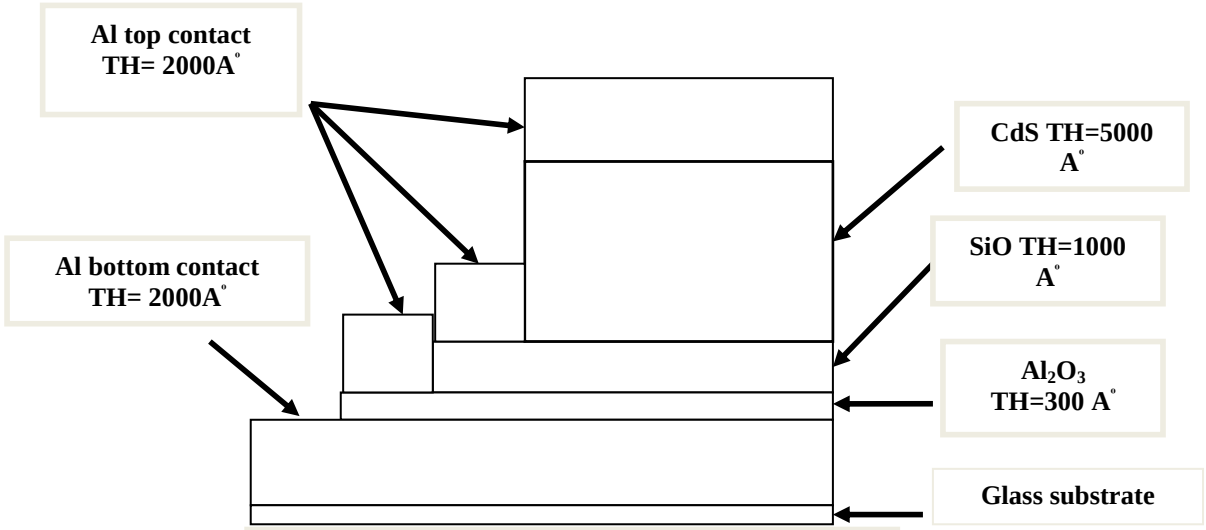


Figure (1). The top view of structure with
(a) Dot gate, (b) strip gate

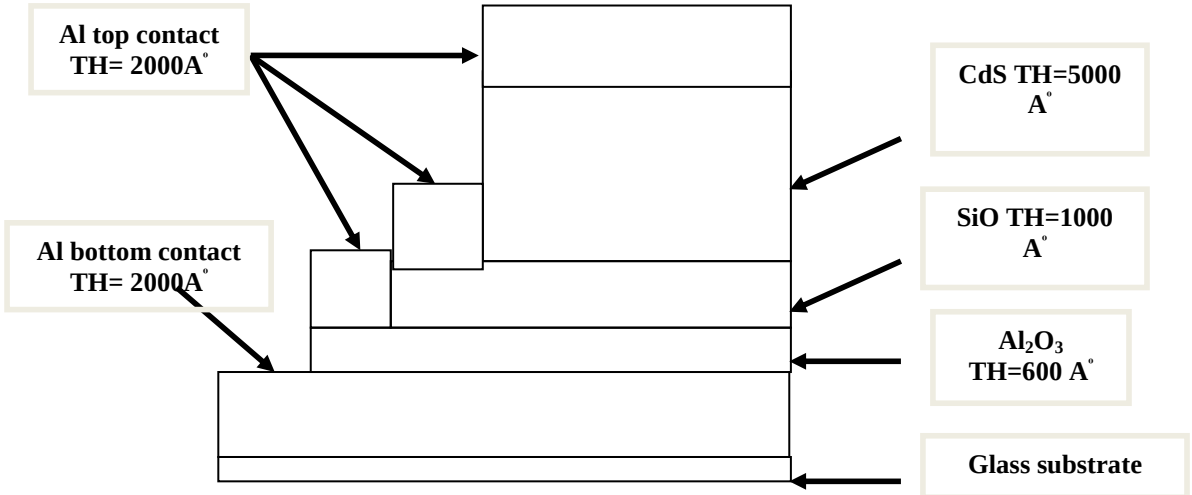
Testing of the first and second (MIOS) structures:

The first structure has been fabricated in figure (2) with thicknesses that Al TH=2000A˚ for top and bottom contacts (metal), Al_2O_3 TH=300A˚ as a second layer (insulator), SiO TH=1000A˚ as a third layer (oxide), and CdS TH=5000A˚as a fourth layer (semiconductor)).



Figure(2)
The first structure

The second structure has been fabricated in figure(3) as same as the first structure except that Al_2O_3 TH= 600A˚ .



Figure(3)
The second structure

After applying the positive and negative biasing voltage, and noting the ON and OFF state for the two kinds of structures, figure (4), (5), (6), (7) show the relationship between the voltage and current for the different structures.

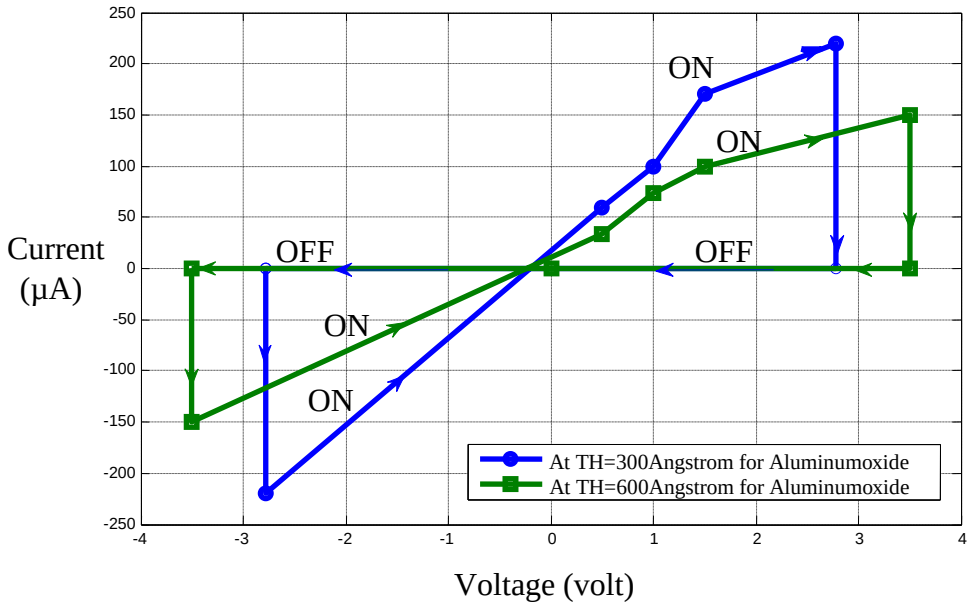


Figure (4)
(I-V) characteristic of Al/Al_2O_3 (metal, insulator, metal) structure with dot gate

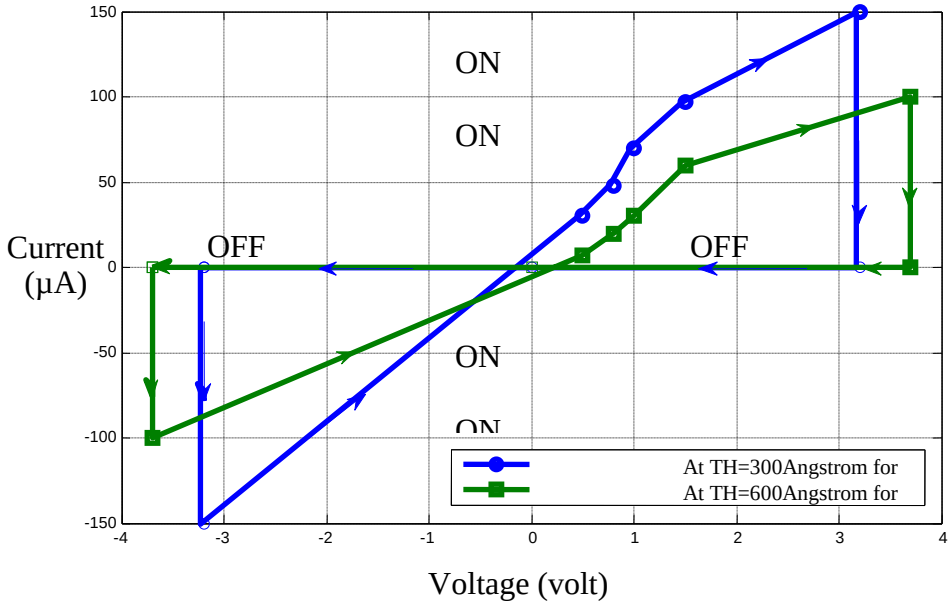


Figure (5)
(I-V) characteristic of Al/Al_2O_3 (metal, insulator, metal) structure with strip gate

It is clear from Figure (4), (6), (dot gate structures), that the switching voltages are 2.78V for Al_2O_3 of 300A˚ thickness and 3.5V for Al_2O_3 of 600A˚ thickness for Al/Al_2O_3 structure, and the currents are (230µA and 150µA) respectively. But for Al/Al_2O_3/SiO structure, the switching voltages are 3.7V for Al_2O_3 of 300A˚ thickness, and 5.3V for Al_2O_3 of 600A˚ thickness, the currents are (220µA and 100µA) respectively. From Figure (5), (7), the switching voltages for (strip gate structures) are 3.2V for Al_2O_3 of 300A˚ thickness and 3.7V for Al_2O_3 of 600A˚ thickness for Al/Al_2O_3 structure, and the currents are (150µA and 100µA) respectively. The switching voltages for Al/Al_2O_3/SiO structure are 4.8V for Al_2O_3 of 300A˚ thickness and 5.8V for Al_2O_3 of 600A˚ thickness, and the currents are (135µA and 95µA) respectively

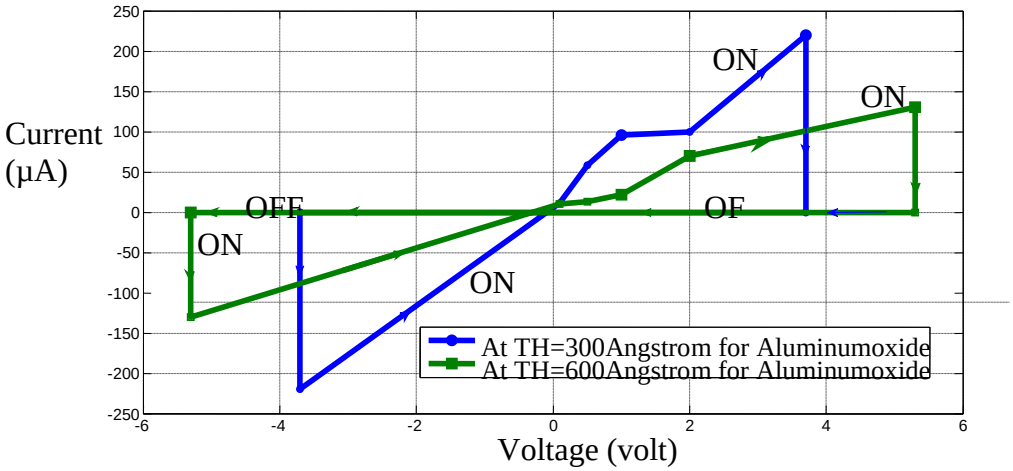


Figure (6)
(I-V) characteristic of Al/Al_2O_3/SiO (metal, insulator, oxide, metal) structure with dot gate

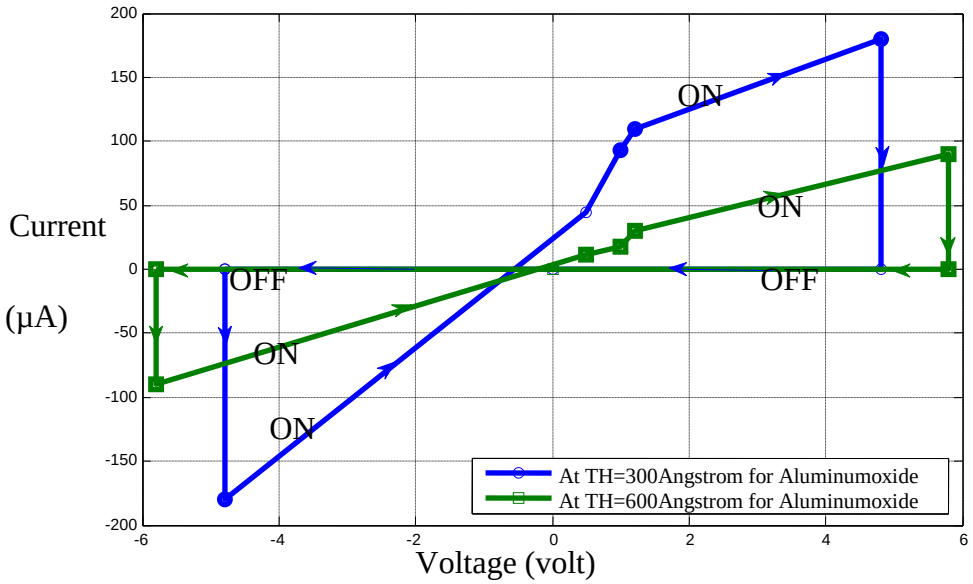


Figure (7)
(I-V) characteristic of Al/Al_2O_3/SiO (metal, insulator, oxide, metal) structure with strip gate

This means that at increasing the thickness of aluminumoxide, the switching voltage for this device is increased; but the current through this insulator is decreased. The thicker oxide induces the higher applied voltage to make the electrons to tunnel the barrier in the structure energy band and then the switching voltage is getting higher [4]. It seemed that reducing the tunnel oxide thickness (Al_2O_3) is a key to lower the operating voltage and/or increasing operating speeds.

The excellent electrical characteristics of memory device need good endurance, long retention time and small operating voltage [5]. The use of an Al_2O_3 dielectric offers several advantages. First, it allows a comparatively simple metal gate integration thus reducing access times. Second, it offers the possibility of a larger design space of the tunnel oxide

thickness; hence the Al_2O_3 is used as a trapping dielectric and control gate dielectric [6]. The increasing of the oxide thickness in some devices applications offers certain advantages, such as longer memory retention, and direct tunneling through the oxide [7].

Figure (8) and Figure (9) show the I-V characteristics of the $Al/Al_2O_3/SiO/CdS$ structure with dot and strip gate.

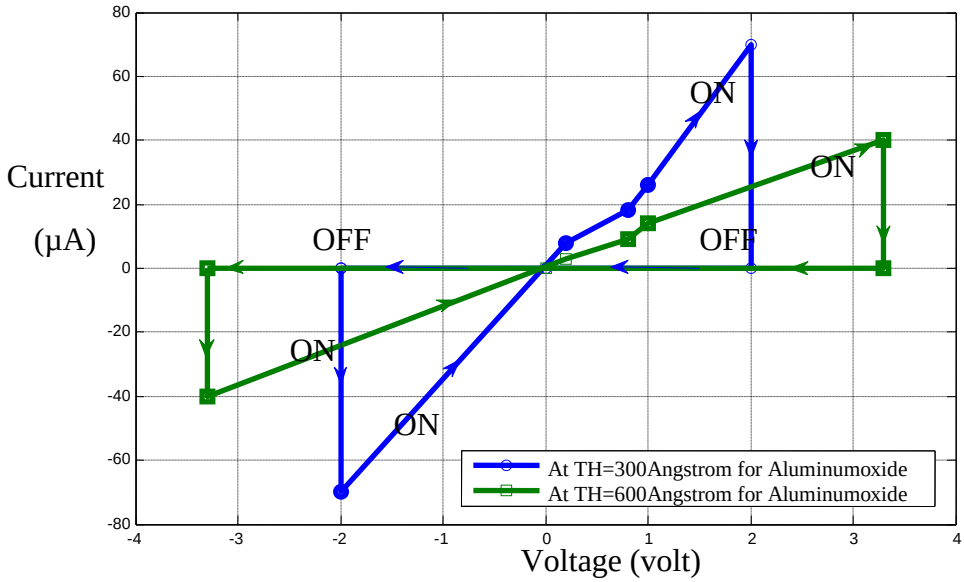


Figure (8)

(I-V) characteristic of $Al/Al_2O_3/SiO/CdS$ (metal, insulator, oxide, semiconductor, metal) structure with dot gate

It is clear that the switching voltage is 2V for Al_2O_3 of 300A˚ thickness, and 3.3V for Al_2O_3 of 600A˚thickness, and the current through these devices is (70µA, and 40µA) respectively. Figure (9) shows the I-V characteristics of similar thickness structure with strip gate. It seems that the switching voltages are 2.5V for Al_2O_3 of 300A˚thickness and 3.8V for Al_2O_3 of 600A˚thickness. But their currents are (60µA,and30µA)respectively. .

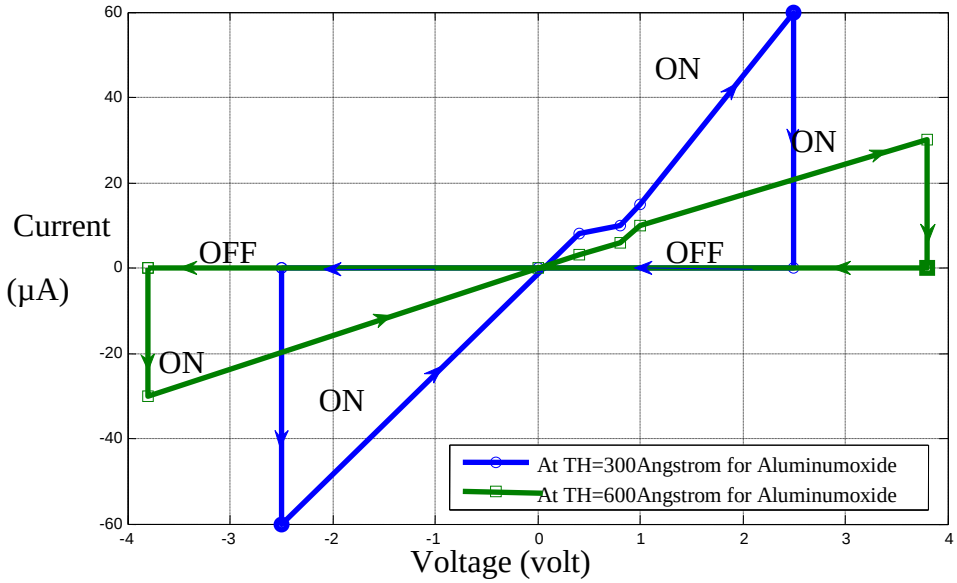


Figure (9) (I-V) characteristic of $Al/Al_2O_3/SiO/CdS$ (metal, insulator, oxide, semiconductor, metal) structure with strip gate

When increasing the thickness of the oxide, the switching voltage is increased also, but the current is decreased through the structure. The same state in strip gate as compared with dot gate.

It has been assumed that the bulk hole traps are distributed almost uniformly in the oxide [8]. A fraction of the generated positive charge is trapped only, because of the recombination of holes with high-density electrons injected from cathode gate metal. It has recently been shown that the increases in low-level leakage currents in thin oxides were no currents flow completely through the oxides. But were; instead, transient currents associated with the charging and discharging of the traps generated by stresses. Thus, the trap generations is responsible for the increases in the interface trap densities and the bulk trap densities were responsible for the increases in the low-level leakage currents, even though these leakage currents in the thin oxides were only due to the transient charging and discharging of stress generated traps [9]. The experimental I-V curves for each device in OFF and ON states are illustrated in figures (4), (5), (6), (7), (8) and figure (9). It is clear from the figures that these devices exhibit memory switching. The ON state is thus retained once the bias is removed giving a non-volatile memory switching. By applying a reverse bias the device can be switched from conducting ON state back to OFF state [10].

Testing of the third (MIOS) structure:

The fifth structure has been deposited in figure (10) with thicknesses that Al TH=2000A˚, CdS TH=5000A˚, Al_2O_3 TH=50A˚, and SiO TH=5000A˚.

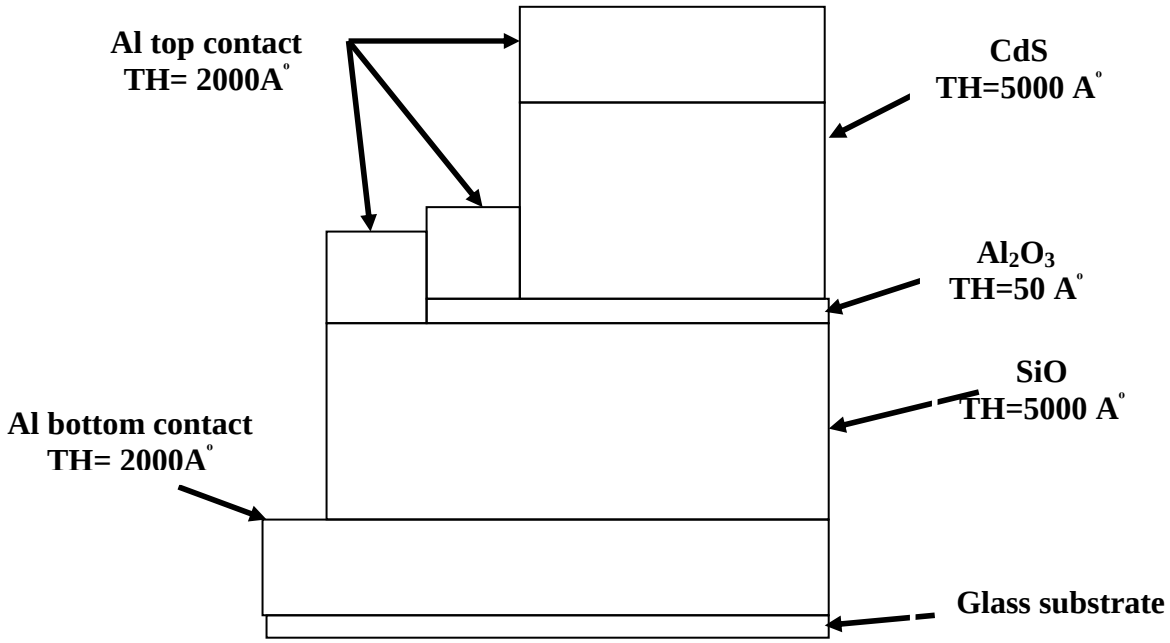


Figure (10) The third structure

Electrons and holes, after being injected through the oxide layer, are trapped into the interface between the two insulators, and in the second insulator layer under application of a large positive and negative stress [11]. As the thickness of oxide is less, the trapped charges between the two insulator interface and in the second insulator will be more because the conduction through thinner oxides is more [8]. When a positive stress=8v for 5 minute is applied to the structure gate, electrons from the depletion region in the substrate at CdS/Al_2O_3interface are assumed to tunnel [10] through the thin oxide layer.

Some of the injected electrons recombine with earlier injected holes. During the positive stress some of the trapped holes may also leave the gate structure due to tunneling. If enough electrons are injected, a net negative charge in the gate structure after removing a pulse is left. In this way, it is possible to shift the flat band voltage to more positive or less negative values (i.e. shift to right). This is illustrated in figure (11) and (12). After applied a positive stress is 1.5V in dot gate and 2.5V in strip gate. After applying a negative stress=-8v for 5 minute, the C-V curve shifts negatively along with voltage axis indicating the presence of the positive charge trapped into the gate structure. This positive charge can be computed from measuring the flat-band voltage shift. The shift window after applying a negative stress is 0.75V for dot gate and 1.2V for strip gate.

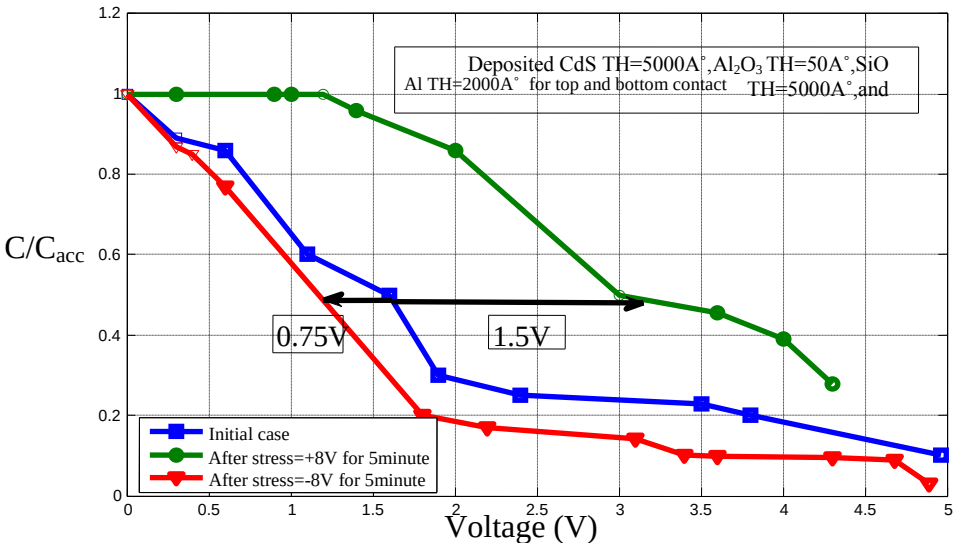


Figure (11)
(C-V) characteristic for dot gate for third structure with stress at duration 5minutes

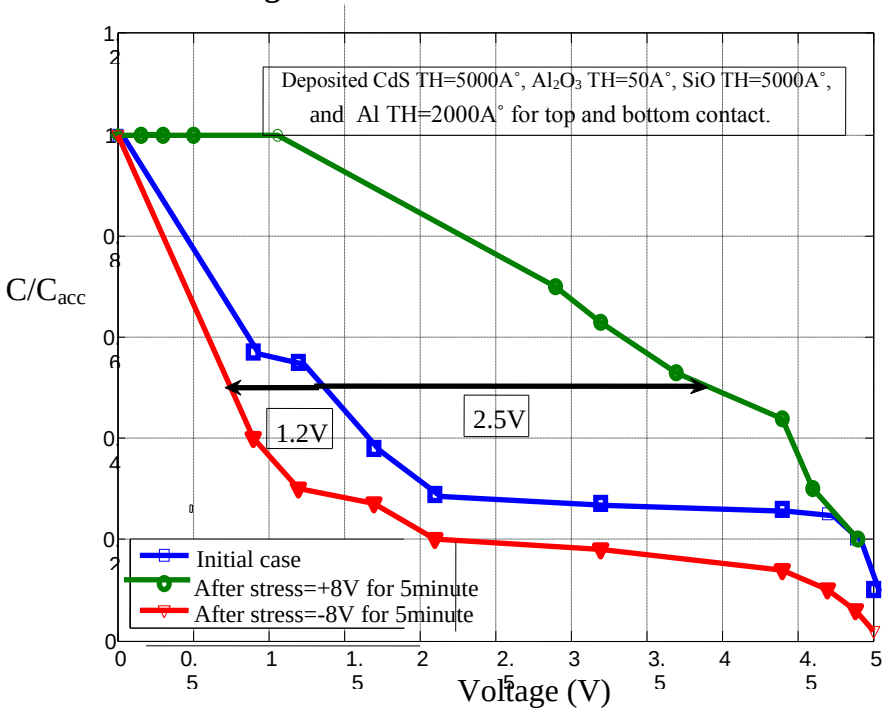


Figure (12)
(C-V) characteristic for strip gate for third structure with stress at duration 5minutes

When decreasing the duration of applied stress, it is found that the shifting window was decreased and the capacitance was decreased also. This is illustrated in figure (13) and figure (14).

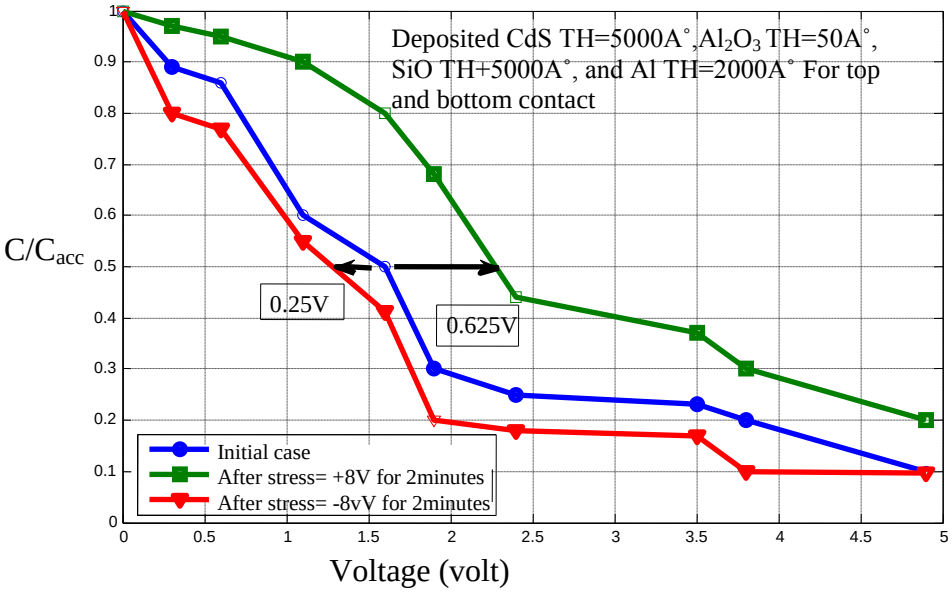


Figure (13)
(C-V) characteristics for dot gate for third structure with stress at duration 2 minutes

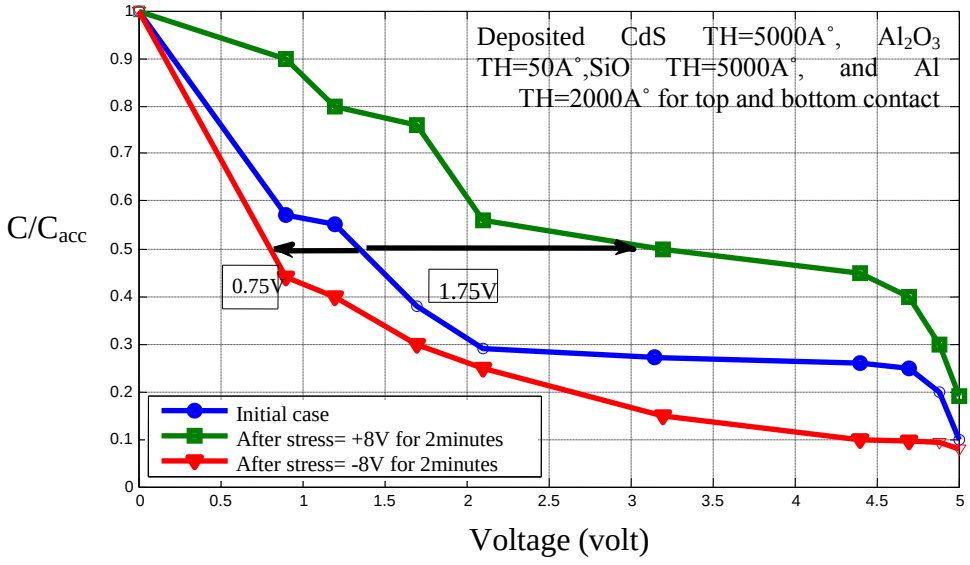


Figure (14)
(C-V) characteristics for strip gate for third structure with stress at duration 2 minutes

When decreasing the duration, the ability of storage in capacitance is decreased also, this is cleared in small value of shifting window at duration 2 minutes.

Conclusions:

The first and second structures operate as memory switching devices. The third reveals as charge storage cells.

The measured characteristics used in this research reveals (I-V) voltage, that at increasing the thickness of aluminumoxide, the switching voltage is increased; but the current through this insulator is decreased. The thicker oxide induces the higher applied voltage to make the electrons to tunnel the barrier in the structure energy band and then the switching voltage is getting higher.

(C-V) characteristics: show the capability of charge storing by applying the bias dc voltage and noticing the capacitance change at various voltages. The capacitance of the thicker oxide is decreased. It is noted that the capacitances of the structures with strip gate are more than the capacitances of the structures with dot gate; this is because the surface area of the strip gate is larger than in the dot gate.

From the C-V curve, it is possible to notice the shifting window by applying the suitable stress voltage for certain time. When a positive stress=8v for 5 minute is applied to the structure gate, electrons from the depletion region in the substrate at CdS/Al_2O_3 interface are assumed to tunnel through the thin oxide layer.

After applying a negative stress=-8v for 5 minute, the C-V curve shifts negatively along with voltage axis indicating the presence of the positive charge trapped into the gate structure. The shift window after applying a negative stress is 0.75V for dot gate and 1.2V for strip gate.

When decreased the duration of applied stress, to 2 minutes, it is found that the shifting window decreases and the capacitance decreases also.

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The work was carried out at the college of Engineering. University of Mosul